Transcend
Exceeding Your Expectations

SDHC Card series

4GB~8GB High Capacity Secure Digital Card

Description

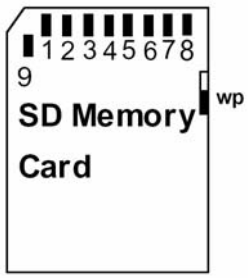
Transcend High Capacity SD Card series are specifically designed to meet the High Capacity, High Definition Audio and Video requirement for the latest Digital Cameras, DV Recorders, Mobile Phones, etc,. The new defined Speed Class enables the host to support AV applications to perform real time recording to the SD memory card.

Features

- ROHS compliant product.
- Card Lid material: PC (comply with UL94,Flame Class:HB)
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Durability: 10,000 insertion/removal cycles
- Compatible with SD Specification Ver. 2.0
- Comply with SD File System Specification Ver. 2.0
- Mechanical Write Protection Switch
- Supports Speed Class Specification up to Class 6
- Supports Copy Protection for Recorded Media (CPRM) for SD-Audio
- Seamless compatibility with SDMI-compliant digital audio devices
- Form Factor: 24mm x 32mm x 2.1mm

Placement

Front



Back

Pin Definition

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT	I/O/PP[3]	Card Detect/Data Line [Bit3]	CS	I	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit2]	RSV		

SDHC Card series

4GB~8GB High Capacity Secure Digital Card

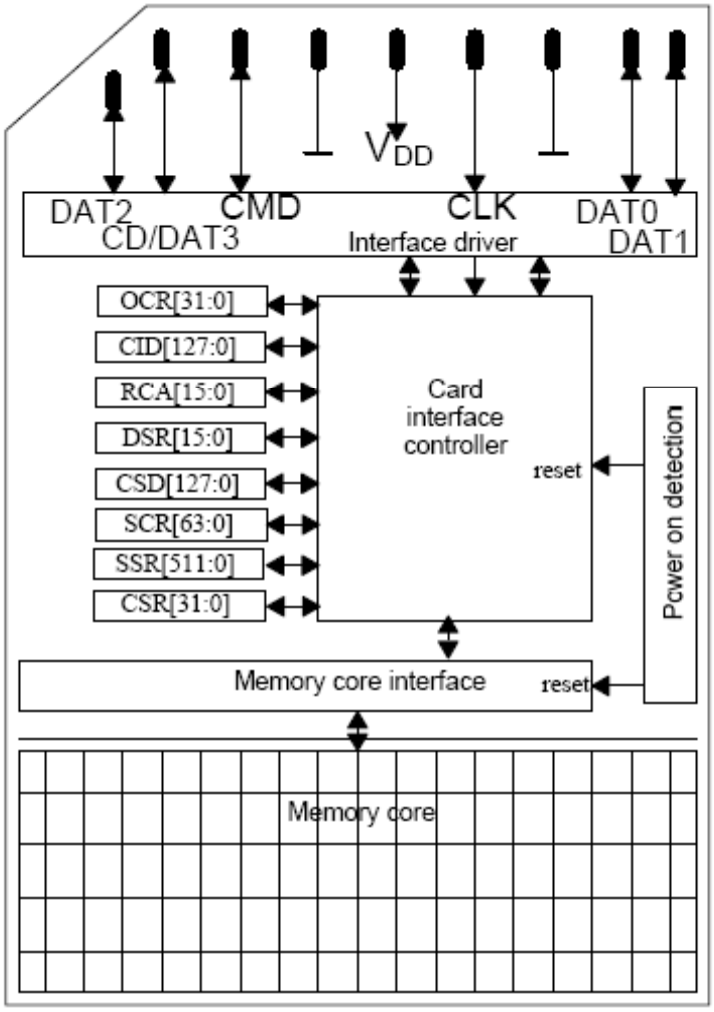
P/N Information

Picture			
Transcend P/N	TS4GSDHC	TS8GSDHC	TS4GSDHC6
Speed Class(1)	CLASS 2	CLASS 2	CLASS 6
Total Area Bytes	4,029,677,568	8,092,385,280	4,062,707,712
User Area Bytes	4,021,288,960	8,083,996,672	4,054,319,104
User Area Sectors	7,854,080	15,789,056	7,918,592
Read Speed (Min.)(2)	18 MB/s	18 MB/s	18 MB/s
Write Speed (Min.)(2)	3.5 MB/s	3.5 MB/s	12 MB/s
Program/Erase Cycles(Min.)	10,000	10,000	100,000
MTBF	> 400,000hr	> 400,000hr	> 1,000,000hr
File System	FAT32	FAT32	FAT32
Weight (g)	2g	2g	2g

(1) Speed Class is determined by TestMatrix Compliance Test, 2.8S

(2) Test Environment:
Processor:Intel Celeron 2.0GHz
Mainboard:MSI 865G
Memory: Transcend DDR266 256M
Card reader: Genesys GL-819 (support SD2.0)
Program: FDbench 1.01

Architecture



Bus Operating Conditions

• General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=-100uA@V_{DD} Min.
Output Low Voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=100uA@V_{DD} Min.
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25* V_{DD}	V	
Power up time			250	ms	From 0v to V_{DD} Min.

• Current Consumption

The current consumption is measured by averaging over 1 second.

- Before first command: Maximum 15 mA
- During initialization: Maximum 100 mA
- Operation in Default Mode: Maximum 100 mA
- Operation in High Speed Mode: Maximum 200 mA
- Operation with other functions: Maximum 500 mA.

• Bus Signal Line Load

The total capacitance C_L the CLK line of the SD Memory Card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:

$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$

Where N is the number of connected cards.

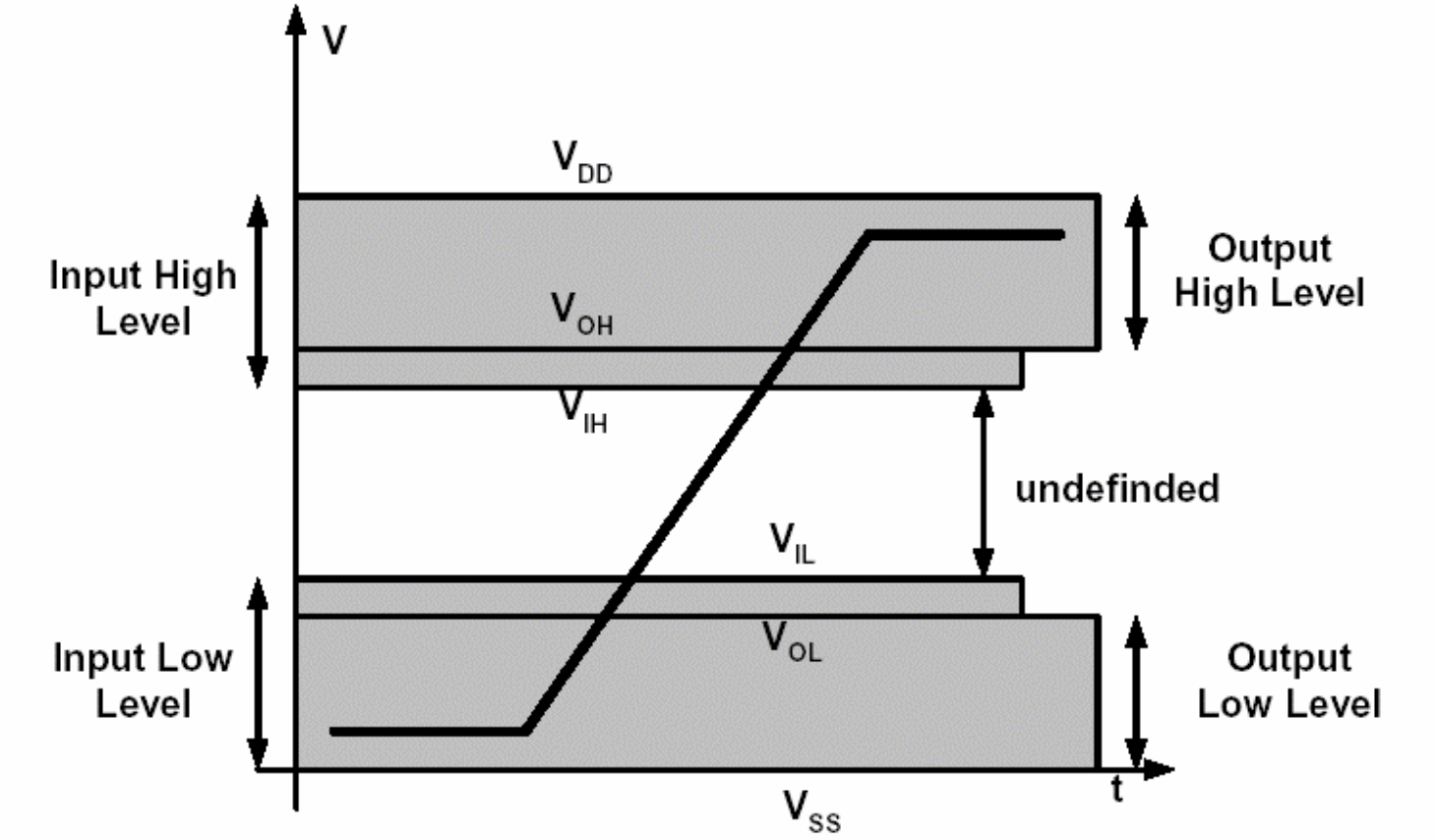
Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Bus signal line capacitance	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF

Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only because they are connected separately to the SD Memory Card host.
Host should consider total bus capacitance for each signal as the sum of C_{HOST}, C_{BUS}, and C_{CARD}, these parameters are defined by per signal. The host can determine C_{HOST} and C_{BUS} so that total bus capacitance is less than the card estimated capacitance load (C_L=40 pF). The SD Memory Card guarantees its bus timing when total bus capacitance is less than maximum value of C_L (40 pF).

• Bus Signal Levels

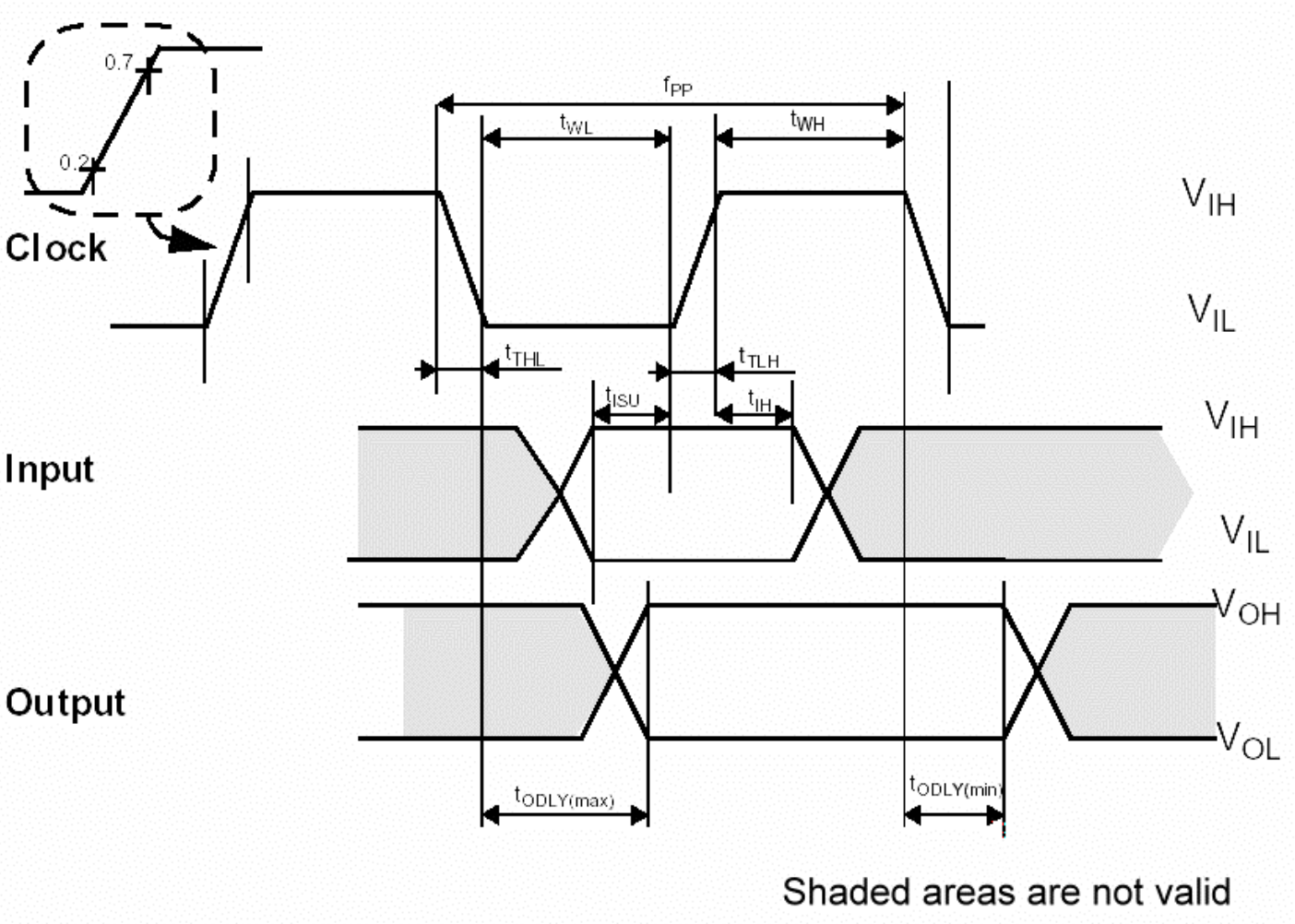
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	0.75* V_{DD}		V	I_{OH} = -100 µA @V_{DD} min
Output LOW voltage	V_{OL}		0.125* V_{DD}	V	I_{OL} = -100 µA @V_{DD} min
Input HIGH voltage	V_{IH}	0.625* V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25* V_{DD}	V	

• **Bus Timing**



Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_{CARD} \leq 10$ pF, (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	KHz	$C_{CARD} \leq 10$ pF, (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leq 10$ pF, (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{CARD} \leq 10$ pF, (1 card)
Input hold time	t_{IH}	5		ns	$C_{CARD} \leq 10$ pF, (1 card)
Outputs CMD, DAT (referenced to CLK)					

Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 40$ pF, (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leq 40$ pF, (1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required

- **Bus Timing (High Speed Mode)**

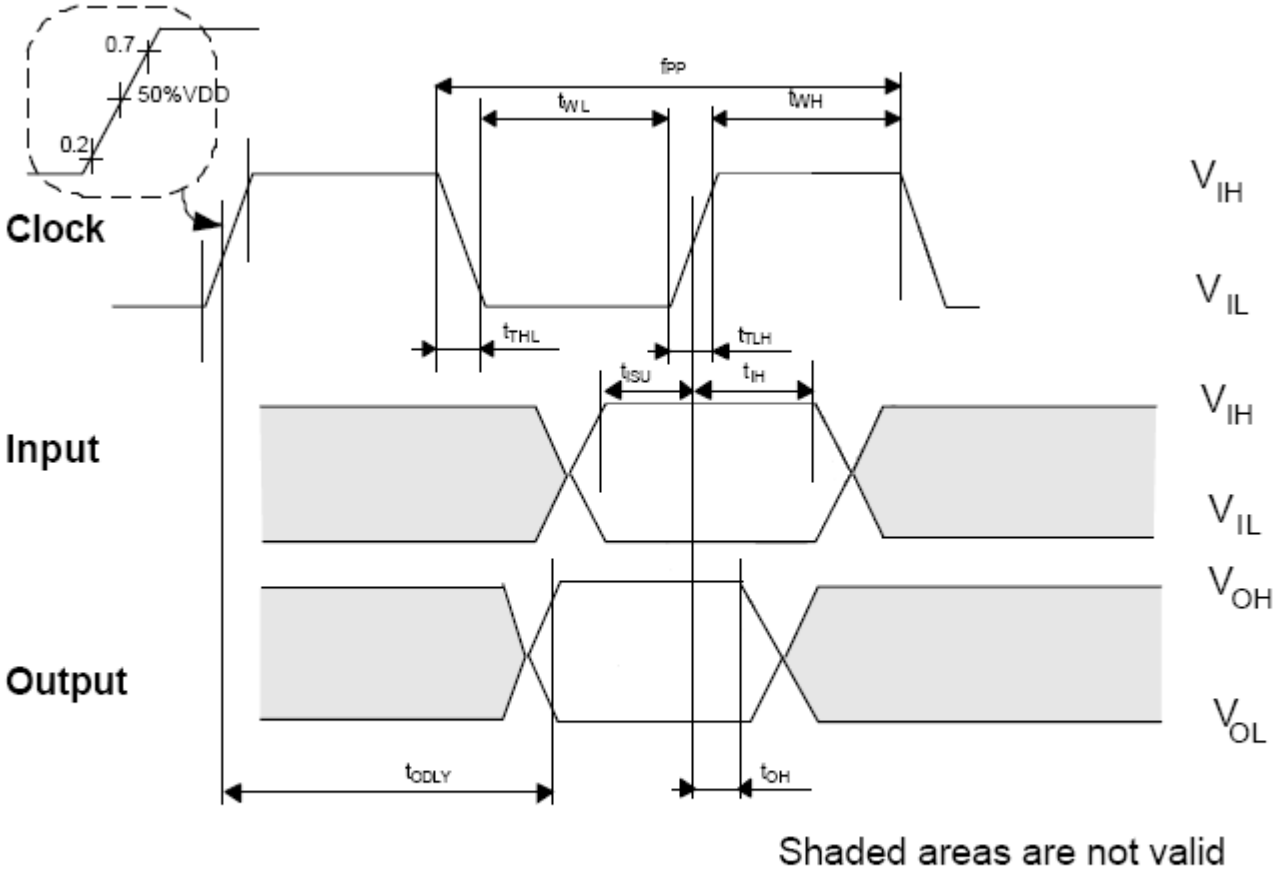


Figure 48: Timing diagram data input/output referenced to clock (High-Speed)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{CARD} \leq 10$ pF, (1 card)
Clock low time	t_{WL}	7		ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock high time	t_{WH}	7		ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{CARD} \leq 10$ pF, (1 card)
Clock fall time	t_{THL}		3	ns	$C_{CARD} \leq 10$ pF, (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{CARD} \leq 10$ pF, (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD} \leq 10$ pF, (1 card)
Outputs CMD, DAT (referenced to CLK)					

Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40$ pF, (1 card)
Output Hold time	t_{OH}	2.5		ns	$C_L \leq 40$ pF, (1 card)
Total System capacitance for each line[1]	C_L		40	pF	(1 card)

1) In order to satisfy severe timing, host shall drive only one card.

Reliability and Durability

Temperature	Operation: -25°C / 85°C (Target spec) Storage: -40°C (168h) / 85°C (500h) Junction temperature: max. 95°C
Moisture and corrosion	Operation: 25°C / 95% rel. humidity Storage: 40°C / 93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10.000 mating cycles; test procedure: tbd.
Bending	10N
Torque	0.15N.m or +/-2.5 deg
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO 7816-1
X-ray exposure	0.1 Gy of medium-energy radiation (70 keV to 140 keV, cumulative dose per year) to both sides of the card, according to ISO7816-1.
Visual inspection Shape and form	No warp page; no mold skin; complete form; no cavities surface smoothness <= -0.1 mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf (Ensures that the WP switch will not slide while it is inserted to the connector.)
WP Switch cycles	minimum 1000 Cycles(@Slide force 0.4N to 5N)

Register Information

Within the card interface six registers are defined: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands (see Chapter 4.7). The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

1. OCR register

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards. The 32-bit operation conditions register stores the VDD voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to 1.

Additionally, this register includes 2 more status information bits. Bit 31 - Card power up status bit, this status bit is set if the card power up procedure has been finished. Bit 30 - Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0 indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card.

The OCR register shall be implemented by the cards.

OCR bit position	OCR Fields Definition	
0-3	reserved	
4	reserved	
5	reserved	
6	reserved	
7	Reserved for Low Voltage Range	
8	reserved	
9	reserved	
10	reserved	
11	reserved	
12	reserved	
13	reserved	VDD Voltage Window
14	reserved	
15	2.7-2.8	
16	2.8-2.9	
17	2.9-3.0	
18	3.0-3.1	
19	3.1-3.2	
20	3.2-3.3	
21	3.3-3.4	
22	3.4-3.5	
23	3.5-3.6	
24-29	reserved	
30	Card Capacity Status (CCS)[1]	
31	Card power up status bit (busy)[2]	

OCR Register Definition

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.

The supported voltage range is coded as shown in Table 5-1. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

2. CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID

An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

• OID

A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

Note: SD-3C, LLC licenses companies that wish to manufacture and/or sell SD Memory Cards, including but not limited to flash memory, ROM, OTP, RAM, and SDIO Combo Cards.
SD-3C, LLC is a limited liability company established by Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation.

• PNM

The product name is a string, 5 ASCII characters long.

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m” is the least significant nibble.
As an example, the PRV binary value field for product revision “6.2” will be: 0110 0010

• PSN

The Serial Number is 32 bits of binary number.

• MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The “m” field [11:8] is the month code. 1 = January.
The “y” field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date “April 2001” will be:
00000001 0100.

• CRC
CRC7 checksum (7 bits).

3. CSD Register
Table 5-16 shows Definition of the CSD for the High Capacity SD Memory Card (CSD Version 2.0). The following sections describe the CSD fields and the relevant data types for the High Capacity SD Memory Card.
CSD Version 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

The CSD Register Fields (CSD Version 2.0)

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

• CSD_STRUCTURE

Field structures of the CSD register are different depend on the Physical Specification Version and Card Capacity.
The CSD_STRUCTURE field in the CSD register indicates its structure version.
The following table shows the version number of the related CSD structure.

CSD_STRUCTURE	CSD structure version	Valid for SD Memory Card Physical Specification Version/Card Capacity
0	CSD Version 1.0	Version 1.01-1.10 Version 2.00/Standard Capacity
1	CSD Version 2.0	Version 2.00/High Capacity
2-3	reserved	

CSD Register Structure

• TAAC

This field is fixed to 0Eh, which indicates 1 ms. The host should not use TAAC, NSAC, and R2W_FACTOR to calculate timeout and should uses fixed timeout values for read and write operations (See 4.6.2).

TAAC bit position	code
2:0	time unit 0=1ns, 1=10ns, 2=100ns, 3=1µs, 4=10µs, 5=100µs, 6=1ms, 7=10ms
6:3	time value 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

• NSAC

This field is fixed to 00h. NSAC should not be used to calculate time-out values.

• TRAN_SPEED

The following table defines the maximum data transfer rate per one data line - TRAN_SPEED:

TRAN_SPEED bit	code
2:0	transfer rate unit 0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s, 3=100Mbit/s, 4... 7=reserved
6:3	time value 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

Note that for current SD Memory Cards that field must be always 0_0110_010b (032h) which is equal to 25MHz - the mandatory maximum operating frequency of SD Memory Card.

In High-Speed mode, that field must be always 0_1011_010b (05Ah) which is equal to 50MHz. And when the timing mode returns to the default by CMD6 or CMD0 command, its value will be 032h.

• CCC

The SD Memory Card command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this card. A value of '1' in a CCC bit means that the corresponding command class is supported.

CCC bit	Supported card command class
0	class 0
1	class 1
.....	
11	class 11

• READ_BL_LEN

This field is fixed to 9h, which indicates READ_BL_LEN=512 Byte.

• READ_BL_PARTIAL

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

• WRITE_BLK_MISALIGN

This field is fixed to 0, which indicates write access crossing physical block boundaries is always disabled in High Capacity SD Memory Card.

• READ_BLK_MISALIGN

This field is fixed to 0, which indicates read access crossing physical block boundaries is always disabled in High Capacity SD Memory Card.

• DSR_IMP

Defines if the configurable driver stage is integrated on the card. If set, a driver stage register (DSR)must be implemented also.

DSR_IMP	DSR type
0	no DSR implemented
1	DSR implemented

• C_SIZE

This field is expanded to 22 bits and can indicate up to 2 TBytes (It is the same as the maximum memory space specified by a 32-bit block address.)
This parameter is used to calculate the user data area capacity in the SD memory card (not include the protected area). The user data area capacity is calculated from C_SIZE as follows: memory capacity = (C_SIZE+1) * 512K byte
As the maximum capacity of the Physical Layer Specification Version 2.00 is 32 GB, the upper 6 bits of this field shall be set to 0.

• ERASE_BLK_EN

This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

• SECTOR_SIZE

This field is fixed to 7Fh, which indicates 64 KBytes. This value does not relate to erase operation. Version 2.00 cards indicates memory boundary by AU size and this field should not be used.

• WP_GRP_SIZE

This field is fixed to 00h. The High Capacity SD Memory Card does not support write protected groups.

• WP_GRP_ENABLE

This field is fixed to 0. The High Capacity SD Memory Card does not support write protected groups.

• R2W_FACTOR

This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout

• WRITE_BL_LEN

This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.

• WRITE_BL_PARTIAL

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

• FILE_FORMAT_GRP

This field is set to 0. Host should not use this field.

• COPY

Defines if the contents is original (= '0') or has been copied (='1'). The COPY bit for OTP and MTPdevices, sold to end consumers, is set to '1' which identifies the card contents as a copy. The COPY bit is an one time programmable bit.

• PERM_WRITE_PROTECT

Permanently protects the whole card content against overwriting or erasing (all write and erase commands for this card are permanently disabled). The default value is '0', i.e. not permanently write protected.

• TMP_WRITE_PROTECT

Temporarily protects the whole card content from being overwritten or erased (all write and erase commands for this card are temporarily disabled). This bit can be set and reset. The default value is '0', i.e. not write protected.

• FILE_FORMAT

This field is set to 0. Host should not use this field.

• CRC

The CRC field carries the check sum for the CSD contents.
The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

The following table lists the correspondence between the CSD entries and the command classes. A '+' entry indicates that the CSD field affects the commands of the related command class.

	Command classes							
CSD Field	0	2	4	5	6	7	8	9
CSD_STRUCTURE	+	+	+	+	+	+	+	+
TAAC		+	+	+	+	+	+	
NSAC		+	+	+	+	+	+	
TRAN_SPEED		+	+					
CCC	+	+	+	+	+	+	+	+

	Command classes							
CSD Field	0	2	4	5	6	7	8	9
READ_BL_LEN		+						
WRITE_BLK_MISALIGN			+					
READ_BLK_MISALIGN		+						
DSR_IMP	+	+	+	+	+	+	+	+
C_SIZE_MANT		+	+	+	+	+	+	
C_SIZE_EXP		+	+	+	+	+	+	
VDD_R_CURR_MIN		+						
VDD_R_CURR_MAX		+						
VDD_W_CURR_MIN			+	+	+	+	+	
VDD_W_CURR_MAX			+	+	+	+	+	
ERASE_BLK_EN				+	+	+	+	
SECTOR_SIZE				+	+	+	+	
WP_GRP_SIZE					+	+	+	
WP_GRP_ENABLE					+	+	+	
R2W_FACTOR			+	+	+	+	+	
WRITE_BL_LEN			+	+	+	+	+	
WRITE_BL_PARTIAL			+	+	+	+	+	
FILE_FORMAT_GRP								
COPY	+	+	+	+	+	+	+	
PERM_WRITE_PROTECT	+	+	+	+	+	+	+	
TMP_WRITE_PROTECT	+	+	+	+	+	+	+	
FILE_FORMAT								
CRC	+	+	+	+	+	+	+	+

4. RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value0x0000 is reserved to set all cards into the *Stand-by State* with CMD7.

5. DSR Register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is

0x404.

6. SCR Register

In addition to the CSD register there is another configuration register that named - SD CARD Configuration Register (SCR). SCR provides information on SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bit. This register shall be set in the factory by the SD Memory Card manufacturer.
The following table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
reserved	-	16	R	[47:32]
reserved for manufacturer usage	-	32	R	[31:0]

• SCR_STRUCTURE

Version number of the related SCR structure in the SD Memory Card Physical Layer Specification.

SCR_STRUCTURE	SCR structure version	SD Physical Layer Specification Version
0	SCR version No. 1.0	Version 1.01-2.00
1-15	reserved	

SCR Register Structure Version

• SD_SPEC

Describes the SD Memory Card Physical Layer Specification version supported by this card.

SD_SPEC	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
3-15	reserved

Physical Layer Specification Version

• DATA_STAT_AFTER_ERASE

Defines the data status after erase, whether it is '0' or '1' (the status is card vendor dependent).

• SD_SECURITY

Describes the security algorithm supported by the card.

SD_SECURITY	Security Specification Version
0	no security
1	Not used
2	Version 1.01
3	Version 2.00
4 .. 7	reserved

SD Supported Security Algorithm

Note that it is mandatory for a regular writable SD Memory Card to support Security Protocol. For ROM (Read Only) and OTP (One Time Programmable) types of the SD Memory Card, the security feature is optional. In the case of Standard Capacity SD Memory Card, this field shall be set to 2 (Version 1.01). In the case of High Capacity SD Memory Card, this field shall be set to 3 (Version 2.00).

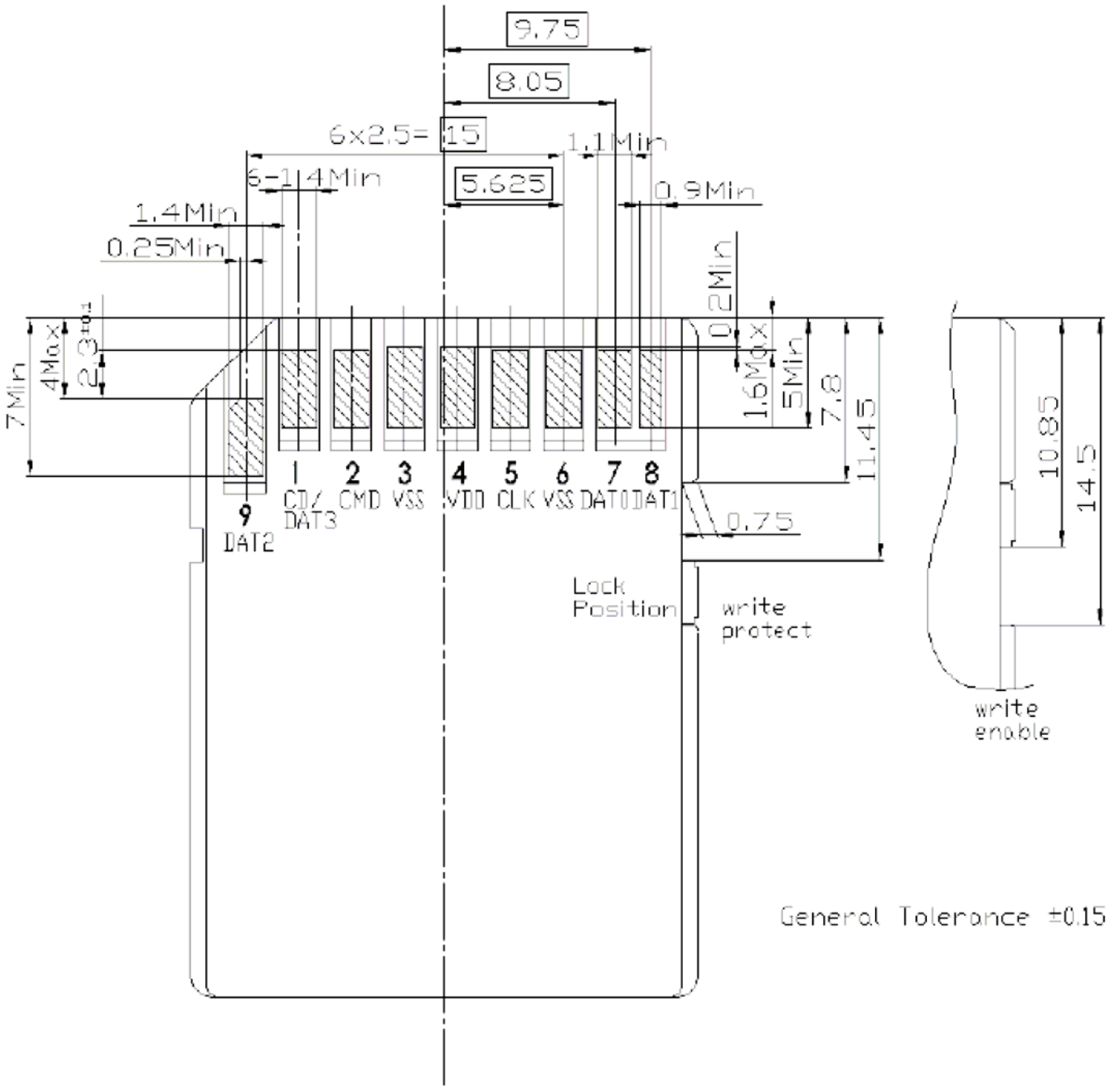
• SD_BUS_WIDTHS

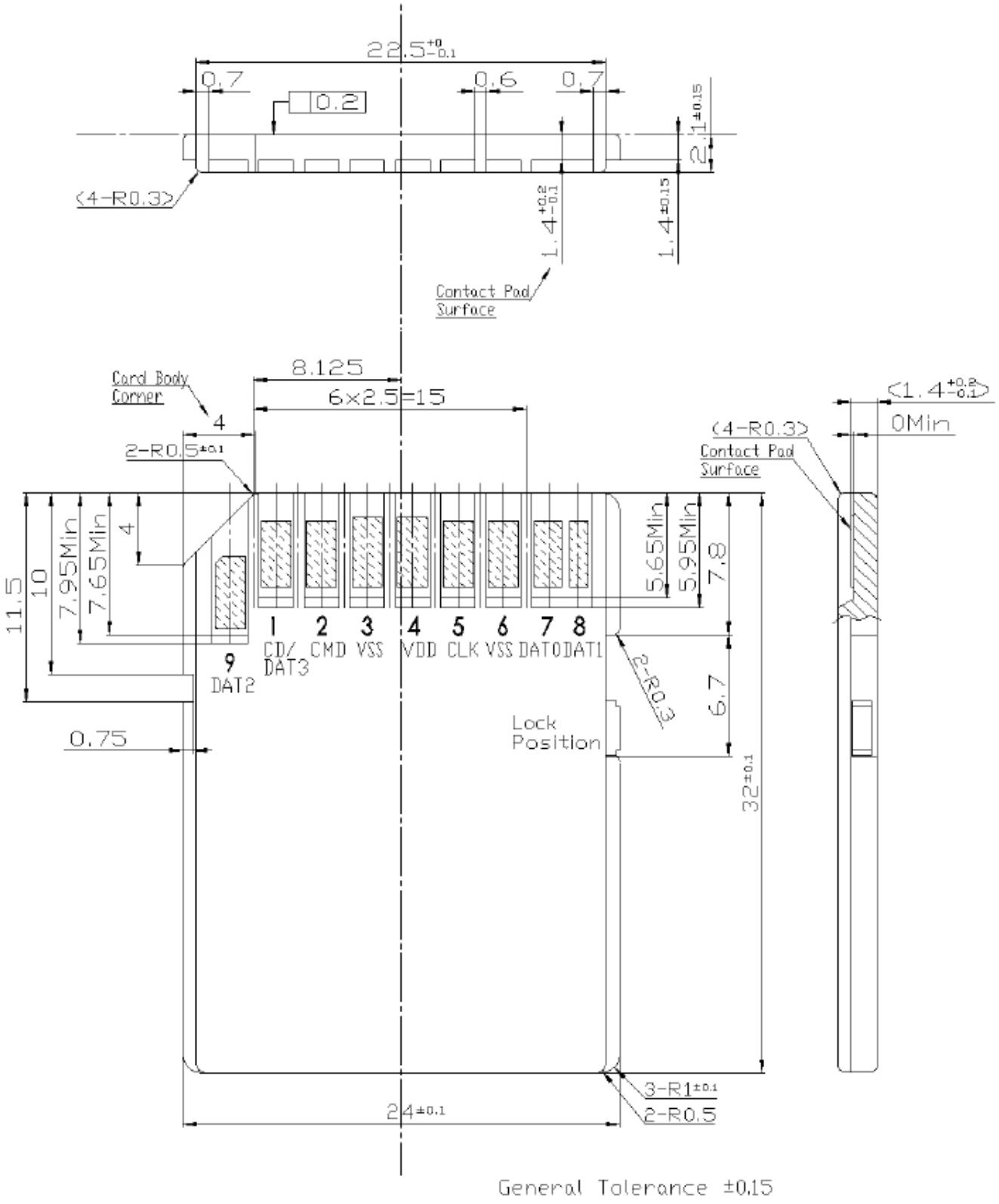
Describes all the DAT bus widths that are supported by this card.

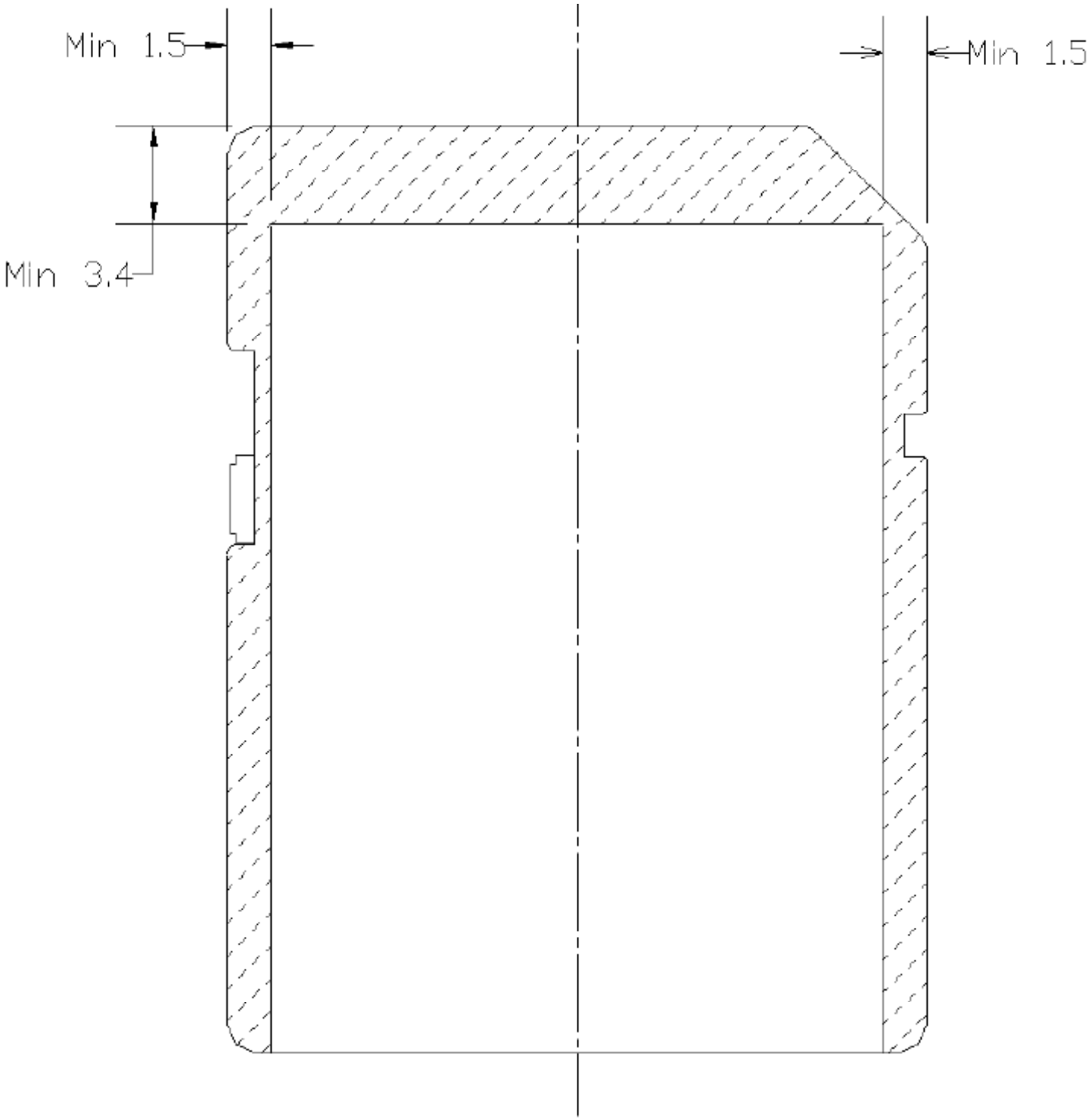
SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit (DAT0)
Bit 1	reserved
Bit 2	4 bit (DAT0-3)
Bit 3 [MSB]	reserved

Since SD Memory Card shall support at least the two bus modes 1bit or 4bit width then any SD Card shall set at least bits 0 and 2 (SD_BUS_WIDTH="0101").

Mechanical Dimension




22.5+0 -0.1
0.7
0.6
0.7
0.2
2.1±0.15
(4-R0.3)
1.4+0.2 -0.1
1.4±0.15
Contact Pad Surface
Card Body Corner
8.125
6×2.5=15
4
2-R0.5±0.1
(1.4+0.8 -0.1)
0Min
(4-R0.3)
Contact Pad Surface
11.5
10
7.95Min
7.65Min
4
5.65Min
5.95Min
7.8
1 2 3 4 5 6 7 8
9
CD/DAT3 CMD VSS VDD CLK VSS DAT0 DAT1
DAT2
2-R0.3
6.7
Lock Position
0.75
32±0.1
3-R1±0.1
2-R0.5
24±0.1
General Tolerance ±0.15


Min 1.5
Min 1.5
Min 3.4